CIAIMS

1. A method of forming an image sensor, comprising:

starting a substrate with a first conductive type of semiconductor material; and

forming a semiconductor layer on the substrate which has a second conductive type;

and

the second conductive type is opposite to the first conductive type and a PN junction is formed in the interface.

2. A method as in claim 1,

the first conductive type semiconductor substrate and the second conductive type semiconductor layer are connecting to different voltage and the said PN junction is reversing biased.

3. A method as in claim 1, further comprising:

forming a photodiode element, the photodiode element having a first well region of said first conductive type formed in said second conductive type semiconductor layer;

a second well region of said second conductive type formed in said second conductive type semiconductor layer but higher doping density compare with said second conductive type semiconductor layer;

and

the said second well region surround the said first well region at first distance and form lateral PN junction

and

the said first well region to said second conductive type semiconductor layer form vertical PN junction

and

both lateral PN junction and vertical junction are reverse biased.

4. A method as in claim 3,

wherein the first distance is between 0.2 micrometer (um) and 3um.

5. A method as in claim 3,

wherein the first depth of the first well region of the first conductive type semiconductor material is about 0.5 um to 3 um and the second depth of the second well region of the second conductive type semiconductor material is about 0.5um to 4 um.

6. A method as in claim 1, further comprising:

forming latch up preventing deep well, a deep well is formed at third center depth and first thickness in said second conductive semiconductor layer below standard N well and standard P well with said second conductive type doping in sensor accessory circuit area to prevent latch up happen.

7. A method as in claim 6,

wherein the third center depth of the deep well is about 1.5um to 3 um, and the first thickness is about 1um to 3 um.

8. A method as in claim 1, further comprising:

growing a top oxide layer; and

after growing a top oxide layer, carrying out a process of chemical mechanical polishing (CMP).

9. A method as in claim 1,

wherein the said first conductive type semiconductor is N type substrate, the said conductive second type semiconductor material layer is a P- type epitaxial layer;

10. A method as in claim 1,

wherein the said first conductive type semiconductor is P type substrate, the said second conductive type semiconductor material layer is a N- type epitaxial layer.

11. A method as in claim 3,

the said first well region can be realized by the standard well forming in standard CMOS process with said first conductive type semiconductor; or realized

by the standard CMOS well stacked with a deep well with said first conductive type semiconductor; and

the said second well region can be realized by the standard well forming in standard CMOS process with said second conductive type semiconductor; or realized by the standard CMOS well stacked with a deep well with said second conductive type semiconductor

13. A method as in claim 1,

wherein the said first type semiconductor substrate doping density is around 10^{14} to 10^{20} atoms/cm3; the said second type semiconductor layer doping density is around 10^{14} to 10^{18} atoms/cm3

14. A method as in claim 1;

the said second type semiconductor layer thickness is around 2um to 12um